REMARKS

Introduction

This is in response to the Office Action dated September 9, 2002 for which a response is due on December 9, 2002.

Claims 55-77 were pending in this application. The examiner examined claims 55-77 in the Office Action dated September 9, 2002. Applicant has amended claim 55 and has amended claims 70-77. Applicant has added new claims 78-89. Therefore, claims 55-89 are pending in the application.

Office Action Dated September 9, 2002

Objection to Drawings

The examiner objected to the drawings under 37 CFR 1.83(a) because, as alleged by the examiner, the drawings fail to show a recessed region as described in the specification. The examiner alleged that the drawings fail to show a recess in the carrier. The examiner pointed out that detail that is essential for proper understanding of the invention should be shown in the drawing pursuant to MPEP 608.02(d). The examiner required correction of the drawing in reply to the office action to avoid abandonment.

Rejection Under 35 USC 112, First Paragraph

The examiner rejected claims 55-77 under 35 USC 112, first paragraph, on the grounds that applicant claimed subject matter that allegedly was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor(s), at the time of the application, had possession of the claimed invention. In claim 55, the examiner referred to the limitation, "said structure is recessed relative to the carrier", and asserted that the specification does not disclose the structure recessed relative to the carrier. The examiner alleged that the written specification only discloses a carrier that includes a recessed region (referring to specification, page 7, lines 7-8). In claims 70 and 74, the examiner referred to the limitation, "a first single crystal silicon wafer layer including a recessed region", and asserted that the specification does not support a first single crystal silicon wafer layer including a recessed

region. The examiner alleged that the specification only discloses a carrier that includes a recessed region.

Double Patenting Rejection

The examiner rejected claims 55-69 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 of U.S. Patent No. 6,316,796.

The examiner rejected claims 70-73 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 39-42 of U.S. Patent No. 6,316,796.

The examiner rejected claims 74-77 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 39-42 of U.S. Patent No. 6,316,796.

Examiner Interview

On or about October 22, 2002, attorney for applicant interviewed the examiner by telephone and discussed the examiner's rejection of the claims under 35 USC 112, first paragraph. Applicant pointed to Figures 9A-9D and Figures 12A-12B and Figure 13 and to the specification, page 26, lines 19-25 as examples for support for a recessed suspended structure in a middle siliccon layer. Applicant's attorney also pointed out that item 247 in Figures 12A-12B is a suspended structure.

Applicant thanks the examiner for taking the time to participate in that interview.

Applicant's Response to the Office Action Dated September 9, 2002

Support For Amendment of Claim 55

Support for amendment to claim 55 as amended is found in claim 55 as originally presented. Claim 55 as originally presented recited, "a single crystal silicon structure formed in said first layer...wherein said structure is recessed relative to the carrier". Claim 55 as amended recites "a first single crystal silicon layer including a recessed region". An example of further support for claim 55 as amended also is found in the specification at page 20, line 14 to page 22,

line 12 which reference Figures 9A-9D. An example of still further support for claim 55 as amended can be found in the specification at page 23, lines 20-29, which explain that the process of Figures 9A-9D can be used to produce any of the suspended structures of Figures 1, 3, 5, 6, 7, 12A-12B or 13, for example.

Support For Amendment of Claims 70-77

Claims 70-77 have been amended to delete phrases with the word "step" so as to remove these claims from consideration under 35 USC 112, sixth paragraph. Applicant chooses to avoid having these claims limited by the narrower scope of protection generally afforded under the means-plus-function rubric.

Support For New Claims 78-89

Applicant respectfully submits that new claims 78-89 find support in the patent specification and claims as originally filed.

In particular, for example, support for claims 78, 80, 81 and 83 is provided in the specification at page 20, line 14 to page 21, line 12 and in Figures 9A-9D. An additional example of support for claims 78, 80, 81 and 83 is provided in the specification at page 26, lines 19-25 and in Figures 12A-12B and 13.

Applicant's Response to Rejection of Drawings

Applicant respectfully traverses the examiner's objection to the drawings. First, there is no need for the drawings to show a recess in the carrier since claims 55-77 as originally presented do not recite a "recess in the carrier" as suggested by the examiner in the objection to the drawing. For instance, the examiner acknowledged in the rejection under 35 USC 112, first paragraph, that claim 55 as originally presented recited "said structure recessed relative to the carrier". Also, for instance, the examiner acknowledged in the rejection under 35 USC 112, first paragraph, that claims 70 and 74 recite the limitation, "a first single crystal silicon wafer layer including a recessed region". Thus, the claims do not recite a "recess in the carrier", and there is no requirement that such recess be shown.

Notwithstanding, the absence of any requirement to show a "recess in the carrier", the drawings do in fact show a recess in the carrier. For example, referring to Figures 8A-8G, there is shown a second wafer having a recessed formed therein. The second wafer serves as a carrier. See specification at page 14, line 18 to page 19, line 13. In particular, please see specification at page 14, line 28 to page 15, line 7 and at page 18, line 7-12.

Applicant's Response to Rejection Under 35 USC 112, First Paragraph

Applicant respectfully traverses the examiner's rejection of claims 55-77 under 35 USC 112, first paragraph.

As to claim 55, the examiner stated that the specification lacks support for the claim 55 limitation, "said structure is recessed relative to the carrier". An example of support in the specification and drawings for this limitation, can be found at page 20, line 14 to page 22, line 12 and in Figures 9A-9D. An example of further support for this limitation can be found in the specification at page 23, line 20 to page 26, line 25 and in Figures 1, 3, 5, 6, 7, 12A-12B and 13. In particular, for instance, please see the specification at page 26, lines 20-23 which states,

> "For example, recesses can be etched in the top and bottom of a middle wafer. The *recessed region* can be etched using DRIE process can be employed to produce the high aspect ratio interleaved plates and high aspect ratio spring structures." (Emphasis added.)

As to claims 70 and 74, the examiner stated that the specification lacks support for the claim 70 and claim 74 limitations, "a first single crystal silicon wafer layer including a recessed region". However, applicant respectfully submits that the portions of the specification and drawings referenced in the above two paragraph of this sub-heading also provide support for the recited language of claims 70 and 74.

Applicant's Response to Obviousness-Type Double Patenting Rejections

Applicant respectfully traverses the examiner's rejection of claims 55-77 under the judicially created doctrine of obviousness type double patenting. Applicant respectfully submits

that claims 55-77, neither as originally presented nor as amended, encompass the subject matter of any of the claims of U.S. Patent No. 6,316,796.

As to claim 55, for example, the examiner correctly pointed out that claim 55 as originally presented recited "said structure is recessed relative to the carrier". In contrast, claims 1-15 of the '796 patent recite "a carrier including a recessed region". Thus, claims 1-15 of the '796 patent recite a carrier that is recessed from the structure, not a structure that is recessed from the carrier. Applicant has made cosmetic changes to the language of claim 55 to make this distinction more apparent.

As to claims 70 and 74, the examiner correctly pointed out that claims 70 and 74 include the limitation, "a first single crystal silicon wafer layer including a recessed region". In contrast, claims 39-42 of the '796 patent recite, "providing a carrier including a recessed region". Thus, claims 39-42 of the '796 patent recite a carrier including a recessed region, not a first single crystal silicon wafer layer including a recessed region.

Amendments to the Specification

Applicant has amended the specification to correct certain typographical errors. No new matter has been added.

Conclusion

Applicant thanks the examiner for his careful examination of the claims of this application. Applicant respectfully requests reconsideration, allowance and passage to issuance of the claims.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**".

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to

charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 356952000304.

Respectfully submitted,

Dated: December 9, 2002 By: _____

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

On page 1, line 4, please add the following new paragraph.

--This invention was made with Government support under Contract No. DAAL01-94-C-3411.--

On page 1, line 8 please replace "higher" with --high--.

The following is a replacement paragraph:

--The invention relates, in general, to semiconductor microelectronic sensors, and more particularly, to single crystal silicon sensors that include structures with diverse contours and [higher] high aspect ratio geometries.--

On page 9, line 26 please replace "is" with --which are--.

The following is a replacement paragraph:

--Moreover, since the processing techniques described below permit deep etching independent of crystallographic directions, the beam 76 and the seismic mass 78 can be formed in (100) silicon wafers [is] which are suitable for fabrication of MOS circuits. Hence, a MOS circuit can be readily formed in the upper face 82 of the seismic mass using standard semiconductor processing techniques.--

On page 12, line 31 please replace "experience" with--experienced--.

The following is a replacement paragraph:

--In operation, the short sense-beam will flex in a direction indicated by arrow 126'. The collection of interdigitated plates 130 and 132 will either experience an increase in overlap capacity or a decrease in overlap capacity depending upon the direction of deflection of the sense-beam 126. Thus, the capacitive plates can be used to sense a degree of deflection of the

sense-beam. Alternatively, the interdigitated beams can be used to apply an electrostatic force sufficient to overcome the deflection of the beam. The degree of electrostatic force necessary to overcome such deflection is related to the acceleration [experience] experienced by the accelerometer 120. The circuitry used to determine the amount of flexure of the sense-beam, and the amount of overlap of the interdigitated plates 130 and 132 or, alternatively, to apply a countervailing electrostatic force, employ techniques well known to those skilled in the art and that are not part of the present invention. Hence they need not be described herein.--

On page 17, line 14, replace the "," after the initial "P" with a ".".

On page 17, line 19 after "region" please insert--)--.

The following is a replacement paragraph:

--In Figure 8F, the first wafer is patterned for a Deep Reactive Ion Etching (DRIE) step which defines the regions of the "top" wafer to be etched. DRIE techniques have become increasingly well known. For example, refer to: V.A. Yunkin, D. Fischer, and E. Voges, "Highly Anisotrophic Selective Reactive Ion Etching of Deep Trenches in Silicon," Microelectronic Engineering, Vol. 23, 1994, at 373-376; C. Linder, T. Tschan, N.F. de Rooij, "Deep Dry Etching Techniques as a New IC Compatible Tool for Silicon Micromachining," Proceedings, Transducers '91, June 1991, at 524-527; C.D. Fund and J.R. Linkowski, "Deep Etching of Silicon Using Plasma," Proceedings of the Workshop on Micromachining and Micropackaging of Transducers, Nov. 7-8, 1984, at 159-164; and J.W. Bartha, J. Greeschner, M. Puech, and P[,]. Maquin, "Low Temperature Etching of Si in High Density Plasma Using $SF_6/0_2$," Microelectronic Engineering, Vol. 27, 1995, at 453-456. Reactive Ion etch equipment now allows the etching of holes or trenches which are very deep (>100 microns), while maintaining high aspect ratios (the ratio between the depth of the etched region and the width of the etched region). It has been found that this equipment is capable of at least 20:1 aspect ratios for trenches as deep as 300 microns.--

On page 21, line 5, delete the second period "." in the sentence ending "214.".

On page 21, line 16, delete "si" and replace with "is".

On page 21, line 17, delete "recesses204" and replace with --recesses 204--.

The following is a replacement paragraph:

--In Figure 9B, a deep reactive ion etch (DRIE) process is employed to produce a high aspect ratio channel 216 which results in a suspended structure 218 surrounded by such high aspect ratio channel 216. The suspended structure 218 is suspended from the lower upstanding structure 212 which is attached to the lower wafer 214. The lower upstanding structure, therefore, anchors a lower end of the suspended structure 218 to the lower wafer 214.[.] The channel 216, for example, can be circular which results in the formation of a generally cylindrical suspended structure 218. It will be appreciated, however, that a circular channel is just one of many possible channel shapes as explained below. Next, an upper wafer 220 is bonded to the wafer 200 enclosing the suspended structure 218 between the upper and lower wafers 220 and 214. The upper upstanding structure 210 has been etched so that its upper or distal end is below the upper surface of the middle wafer 200. As a result, when the uppper wafer 220 is bonded to the middle wafer 200, there is a gap between the upper upstanding structure 210 and the upper wafer 220. An upper or distal end of the suspended structure 218, is not unattached to the upper wafer 220 and is free to move about. The suspended structure 218 [si] <u>is</u> disposed within a cavity defined by the etched [recesses204] <u>recesses 204</u> and 206 and by the DRI etched channel 216. The lower upstanding structure 212 anchors the suspended structure 218 to the lower wafer 214 within the cavity. As illustrated in figures 1, 3, 6, 12A-12B and 13, the lower upstanding structure 212 can be constructed to be a flexible member, such as a spring or a beam, for sensor or actuator applications. Also, the suspended structure 218 may be encapsulated in an environment, gaseous or near vacuum, in which the bonding of the upper wafer 220 may take place.--

On page 22, line 26 please replace " in," with --, in--.

The following is a replacement paragraph:

As an alternative to the overall fabrication process described above with respect to Figures 9A-9D, instead of forming recesses in a middle wafer, recesses could be formed in upper and lower (outer) wafers. For example, referring to the illustrative drawings of Figure 10, there is shown a side cross-sectional view of an alternative multiple wafer device with an SCS released structure 218". Upper and lower wafers 220' and 214' have recesses formed in them as shown. The recess in the upper wafer 220' and 214' have recesses formed in them as shown. The recess in the upper wafer 220' defines an upper upstanding structure 210'. The recess 206' in the lower wafer 214' defines a lower upstanding structure 212'. A middle wafer 200' that has a channel 216' formed by a deep reactive ion etch is bonded between the upper and lower wafers 214' and 220'. Thus, the released structure 218' is disposed within a cavity defined by the etched recesses 204' and 206' and by the DRI etch channel 216'. The actual process steps, in[,] accordance with the invention, that produce the structure of Figure 10 will be appreciated by those of ordinary skill in the art from the explanation above relative to Figures 9A-9D and need not be set forth in detail herein.--

On page 23, line 15 please replace " in," with --, in--.

The following is a replacement paragraph:

--Another alternative to the overall fabrication process described above involves the etching through both upper and lower wafers in order to release a structure formed from a middle wafer. Referring to the illustrative drawing of Figure 11, for example, there is shown a side cross-sectional view of another alternative multiple wafer device with an SCS released structure 218". The middle wafer 200" is etched in a manner similar to the wafer 200 of Figures 9A-9D. In particular, a channel 216" is formed by deep reactive ion etching. However, an upper upstanding structure 210" of the wafer 200" of Figure 11 is bonded to an upper wafer 200".

Hence, in order to release the structure 218", a channel 222" is etched in a lower wafer 214", and a channel 228" is etched in the upper wafer 220". The actual process steps, in[,] accordance with the invention, that produce the structure of Figure 11 will be appreciated by those of ordinary skill in the art from the explanation above relative to Figures 9A-9D and need not be set forth in detail herein.--

On page 39, line 10 before "semiconductor" please insert --a--.

The following is a replacement paragraph:

--In one aspect, the invention provides a semiconductor sensor which includes a first single crystal silicon wafer layer. A single crystal silicon structure is formed in the first wafer layer. The structure includes two oppositely disposed substantially vertical major surfaces and two oppositely disposed generally horizontal minor surfaces. The aspect ratio of major surface to minor surface is at least 5:1. A carrier which includes a recessed region is secured to the first wafer layer such that said structure is suspended opposite the recessed region.--

In the Claims:

Please amend claim 55 and claims 70-77 as follows.

55. (Once Amended) A semiconductor micromechanical device comprising:

a first single crystal silicon wafer layer including a recessed region;

a single crystal silicon structure formed in said recessed region of the first layer and including two oppositely disposed substantially vertical major surfaces and including two oppositely disposed generally horizontal minor surfaces wherein the aspect ratio of major surface to minor surface is at least 5:1; and

a carrier secured to said first wafer layer[;

wherein said structure is recessed relative to the carrier] such that said structure is suspended opposite the carrier.

70. (Once Amended) A semiconductor micromechanical device produced by[the steps of]:

providing a first single crystal silicon wafer layer including a recessed region;

providing a carrier;

securing the first wafer layer to the carrier with the recessed region facing the carrier; and

etching substantially vertically through the first wafer layer near the recessed region so as to form a beam integral with the first wafer layer and suspended over the carrier wherein the beam has an aspect ratio of height to width of at least 5:1.

71. (Once Amended) The micromechanical device of claim 70 wherein [the step of] etching includes reactive ion etching.

72. (Once Amended) The micromechanical device of claim 70 wherein [the step of] providing the first wafer layer includes providing a single crystal (100) oriented silicon wafer layer.

73. (Once Amended) The micromechanical device of claim 70 wherein [the step of] etching includes etching substantially vertically through the first wafer layer near the recessed region so as to form multiple beams integral with the first wafer layer and suspended over the recessed region wherein each beam has an aspect ratio of height to width of at least 10:1.

74. (Once Amended) A semiconductor micromechanical device produced by [the steps of]:

providing a first single crystal silicon wafer layer including a recessed region;

providing a carrier;

fusion bonding the first wafer layer to the carrier with the recessed region facing the carrier; and

etching substantially vertically through the first wafer layer near the recessed region so as to form a plate integral with the first wafer layer and suspended over the carrier wherein the plate has an aspect ratio of height to width of at least 5:1.

75. (Once Amended) The micromechanical device of claim 74 wherein [the step of] etching includes reactive ion etching.

76. (Once Amended) The micromechanical device of claim 74 wherein [the step of] providing the first wafer layer includes providing a single crystal (100) oriented silicon wafer layer.

77. (Once Amended) The micromechanical device of claim 74 wherein [the step of] etching includes etching substantially vertically through the first wafer layer near the recessed region so as to form multiple plates integrated with the first wafer layer and suspended over the carrier wherein each plate has an aspect ratio of height to width of at least 10:1.

Please add the following new claims 78-89.

--78. (New) The semiconductor micromechanical device of claim 55,

wherein the first silicon layer includes an upper surface including an upper recess and a lower surface including a lower recess that define the recessed region.--

--79. (New) The semiconductor micromechanical device of claim 55,

wherein the carrier comprises a silicon wafer layer.--

--80. (New) The semiconductor micromechanical device of claim 55,

wherein the first silicon layer includes an upper surface including an upper recess and a lower surface including a lower recess that define the recessed region, further including:

an upper silicon layer secured to the upper surface of the first silicon layer opposite the upper recess in the upper surface of the first silicon layer; and

wherein the carrier is secured to the lower surface of the first silicon layer opposite the lower recess of the lower surface of the first silicon layer.--

--81. (New) The semiconductor micromechanical device of claim 55,

wherein the first silicon layer includes an upper surface including an upper recess and a lower surface including a lower recess that define the recessed region, further including:

an upper silicon layer secured to the upper surface of the first silicon layer opposite the upper recess in the upper surface of the first silicon layer;

wherein the carrier comprises a lower silicon layer; and

wherein the carrier is secured to the lower surface of the first silicon layer opposite the lower recess of the lower surface of the first silicon layer.--

--82. (New) The semiconductor micromechanical device of claim 55,

wherein the aspect ratio of major surface to minor surface of the structure is at least 10:1.--

--83. (New) A semiconductor micromechanical device comprising:

a first single crystal silicon layer including an upper surface including an upper recess and a lower surface including a lower recess that define a recessed region;

a single crystal silicon structure formed in the recessed region of the first layer and including two oppositely disposed substantially vertical major surfaces and including two oppositely disposed generally horizontal surfaces wherein the aspect ratio of major surface to minor surface is at least 5:1; and

an upper silicon layer secured to the upper surface of the first silicon layer opposite the upper recess in the upper surface of the first silicon layer; and

a lower silicon layer secured to the lower surface of the first silicon layer opposite the lower recess in the lower surface of the first silicon layer.--

--84. (New) The semiconductor micromechanical device of claim 83,

wherein the upper silicon layer and the first silicon layer are fusion bonded together; and

wherein the lower silicon layer and the first silicon layer are fusion bonded together.--

--85. (New) The semiconductor micromechanical device of claim 83,

wherein the first layer is formed of (100) oriented silicon crystal.--

--86. (New) The semiconductor micromechanical device of claim 83, wherein the structure is a beam secured at only at only one thereof to the first layer.--

--87. (New) The semiconductor micromechanical device of claim 83, wherein the aspect ratio of major surface to minor surface of the structure is at least 10:1.--

--88. (New) The semiconductor micromechanical device of claim 83, wherein the aspect ratio of major surface to minor surface of the structure is at least 20:1.--

--89. (New) The semiconductor micromechanical device of claim 83, wherein the structure is a beam secured at only one end thereof to the first layer and includes a seismic mass at another other end thereof.--